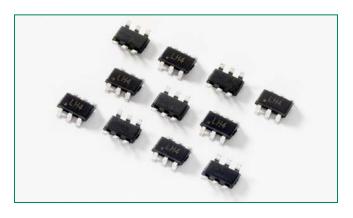


RoHS



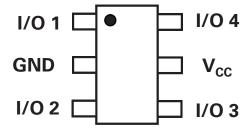
SP3050 Lead-Free/Green Series



Description

The SP3050 integrates low capacitance rail-to-rail diodes with an additional zener diode to protect each I/O pin against ESD and high surge events. This robust device can safely absorb surge current per IEC61000-4-5 ($t_{\rm p}\!=\!8/20\mu s$) without performance degradation and a minimum $\pm 20kV$ ESD per IEC61000-4-2. Their very low loading capacitance also makes them ideal for protecting high speed signal pins.

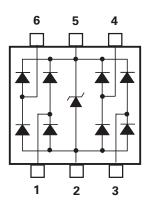
Pinout



Features

- ESD, IEC61000-4-2, ±20kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 10A (8/20µs)
- Low capacitance of 2pF (TYP) per I/O
- Low leakage current of 0.5µA (MAX) at 5V
- Small SOT23-6 packaging

Functional Block Diagram



Applications

- LCD/PDPTVs
- Monitors

1

- Notebooks
- 10/100/1000 Ethernet
- Firewire
- Set Top Boxes
- Flat Panel Displays
- Portable Medical

SPA™ Silicon Protection Array Products Low Capacitance Diode Array for ESD and Surge Protection



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I _{PP}	Peak Current (t _p =8/20µs) ¹	10.0	А
T _{OP}	Operating Temperature	-40 to 85	°C
T _{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Reverse Standoff Voltage V _{RWM}		I _R ≤ 1μA			6.0	V
Reverse Leakage Current I _{LEAK}		V _R =5V		0.1	0.5	μΑ
	V _c	I_{pp} =1A, t_p =8/20 μ s, I/O to GND ²		8.8	10.0	V
Clamp Voltage ¹		I_{pp} =5A, t_p =8/20 μ s, I/O to GND ²		11.5	13.0	V
		I_{pp} =8A, t_p =8/20 μ s, I/O to GND ²		13.2	15.0	V
ESD Withstand Voltage ¹	\/	IEC61000-4-2 (Contact)	±20			kV
L3D Withstand Voltage	V _{ESD}	IEC61000-4-2 (Air)	±30			kV
Diode Capacitance ¹	C _{VO GND}	Reverse Bias=0V		2.4	3.0	pF
Diode Capacitance		Reverse Bias=1.65V		2.0		pF
Diode Capacitance ¹ C _{I/O-I/O} Reverse Bias=0V			1.2		pF	

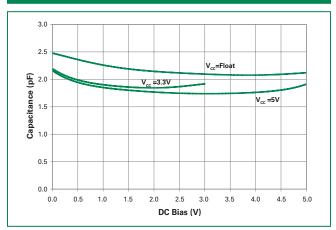
Notes: ¹ Parameter is guaranteed by design and/or device characterization.

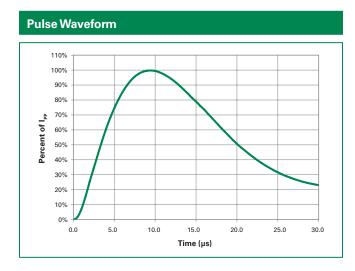
¹Non-repetitive pulse per waveform on page 3

² Repetitive pulse per waveform on page 3.

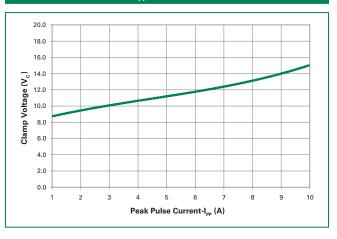


Capacitance vs. Reverse Bias





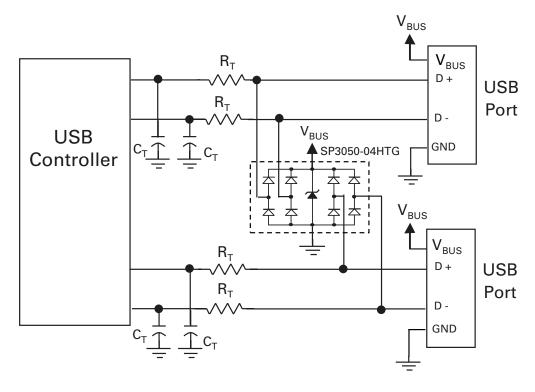
Clamping Voltage vs. Ipp



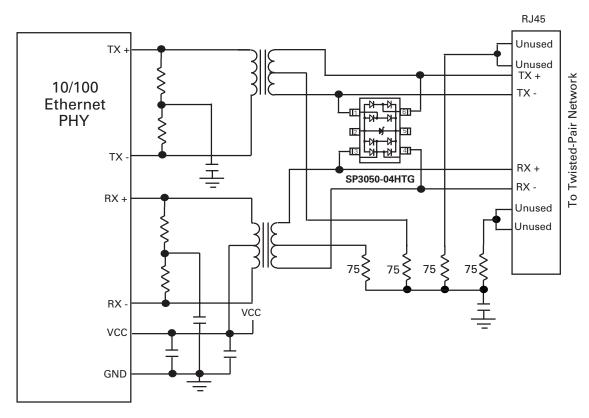


Application Example

Dual Port Protection



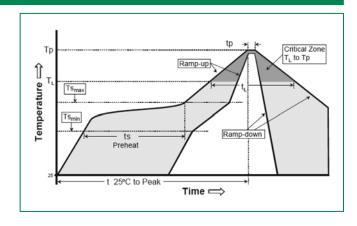
10/100 Ethernet Differential Protection



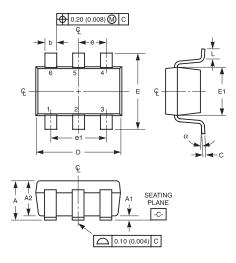


Soldering Parameters

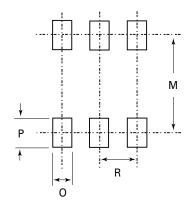
Reflow Condition		Pb – Free assembly	
Pre Heat	-Temperature Min (T _{s(min)})	150°C	
	-Temperature Max (T _{s(max)})	200°C	
	-Time (min to max) (t _s)	60 – 180 secs	
Average ramp up rate (Liquidus) Temp (T _L) to peak		3°C/second max	
T _{S(max)} to T _L - Ramp-up Rate		3°C/second max	
Reflow	-Temperature (T _L) (Liquidus)	217°C	
	-Temperature (t _L)	60 – 150 seconds	
PeakTemperature (T _P)		250 ^{+0/-5} °C	
Time within 5°C of actual peak Temperature (t _p)		20 – 40 seconds	
Ramp-down Rate		6°C/second max	
Time 25°C to peak Temperature (T _p)		8 minutes Max.	
Do not exceed		260°C	



Package Dimensions - SOT23-6



Recommended Solder Pad Layout



Package	SOT23-6				
Pins	6				
JEDEC	MO-203 Issue A				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	Notes
Α	0.900	1.450	0.035	0.057	-
A1	0.000	0.150	0.000	0.006	-
A2	0.900	1.300	0.035	0.051	-
b	0.350	0.500	0.0138	0.0196	-
С	0.080	0.220	0.0031	0.009	-
D	2.800	3.000	0.11	0.118	3
E	2.600	3.000	0.102	0.118	-
E1	1.500	1.750	0.06	0.069	3
е	0.95 Ref		0.0374 ref		-
e1	1.9 Ref		0.074	8 Ref	-
L	0.100	0.600	0.004	0.023	4,5
N	6		6		6
а	0°	10°	0°	10°	-
M		2.590		0.102	-
0		0.690		.027 TYP	-
P		0.990		.039 TYP	-
R		0.950		0.038	-

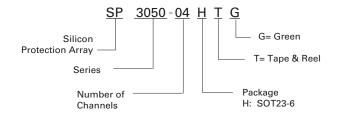
Notes:

- 1. Dimensioning and tolerances per ANSI 14.5M-1982.
- 2. Package conforms to EIAJ SC-74 (1992).
- 3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
- 4. Footlenth L measured at reference to seating plane.
- 5. "L" is the length of flat foot surface for soldering to substrate.
- 6. "N" is the number of terminal positions.
- Controling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

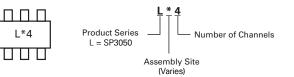
SPA™ Silicon Protection Array Products Low Capacitance Diode Array for ESD and Surge Protection



Part Numbering System



Part Marking System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :

- 1. All dimensions are in millimeters
- 2. Dimensions include solder plating.
- 3. Dimensions are exclusive of mold flash & metal burr.
- 4. All specifications comply to JEDEC SPEC MO-223 Issue A
- 5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
- 6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3050-04HTG	SOT23-6	L*4	3000



Embossed Carrier Tape & Reel Specification -- SOT23-6

8mm TAPE AND REEL

